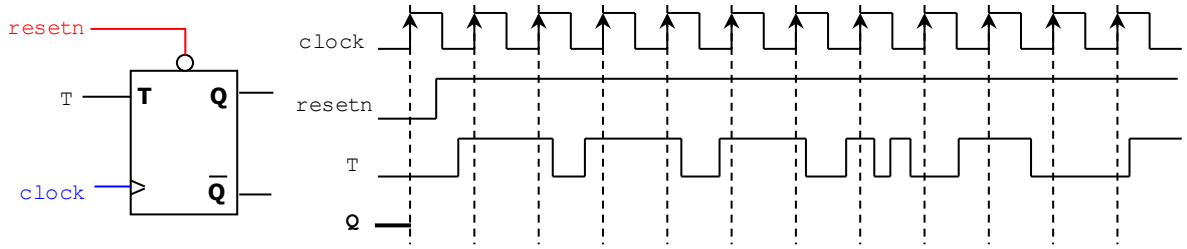
Homework 3

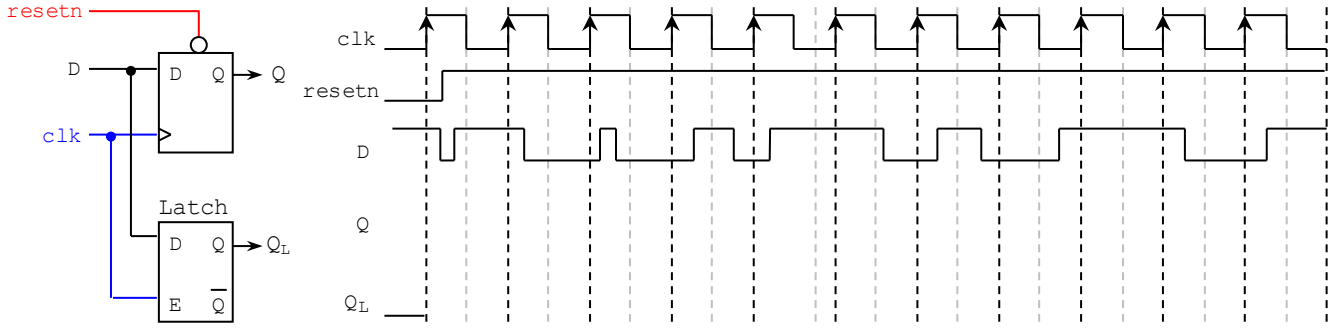
(Due date: March 14th @ 5:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (12 PTS)

- Complete the timing diagram of the circuit shown below. (5 pts)

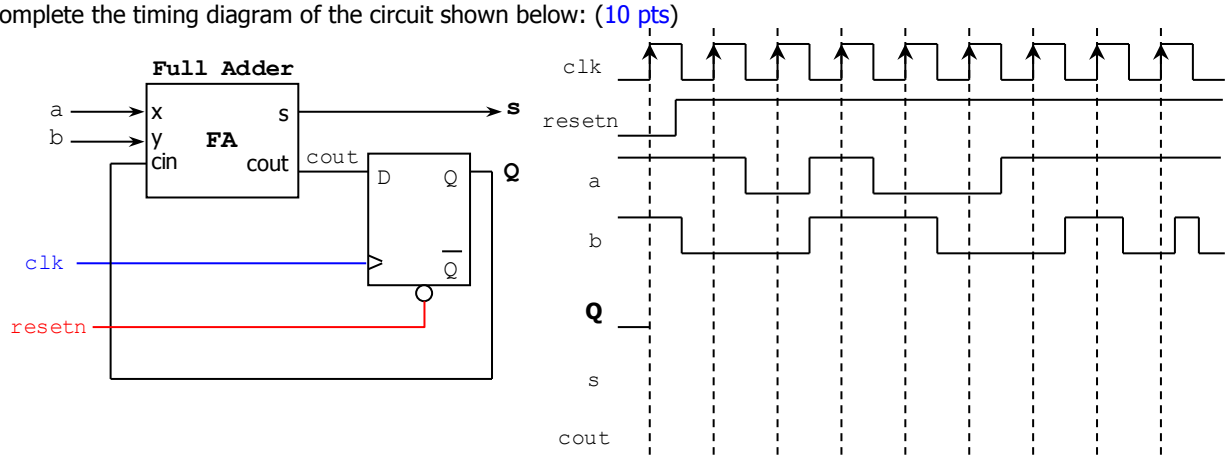


- Complete the timing diagram of the circuits shown below: (7 pts)

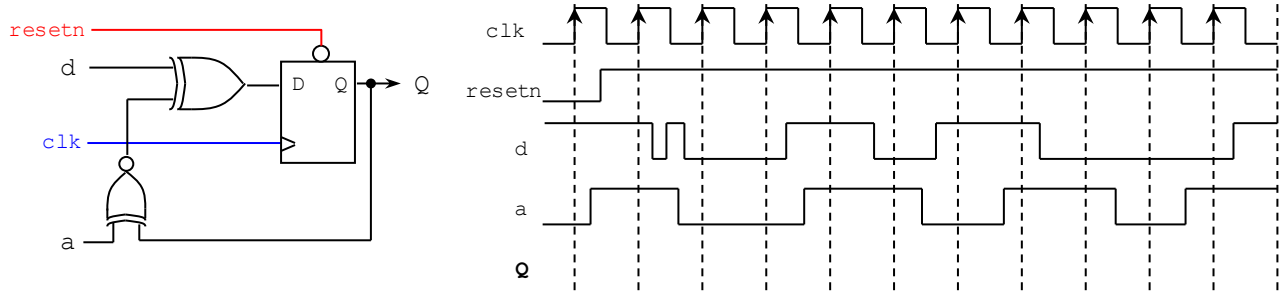


PROBLEM 2 (33 PTS)

- Complete the timing diagram of the circuit shown below: (10 pts)

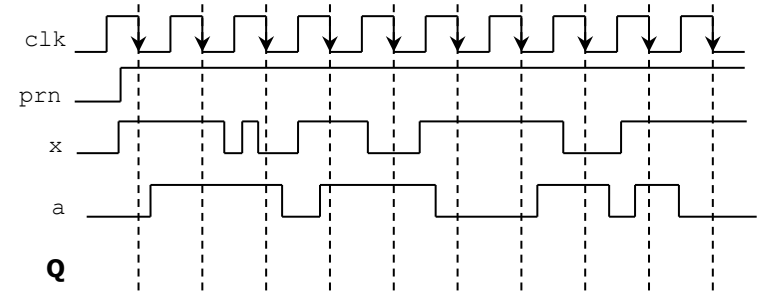


- Complete the timing diagram of the circuit shown below: (7 pts)

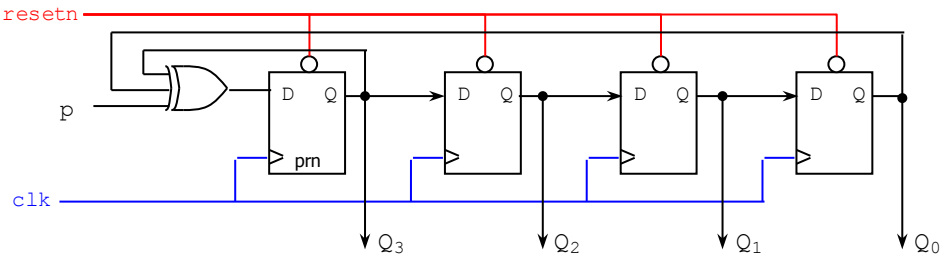


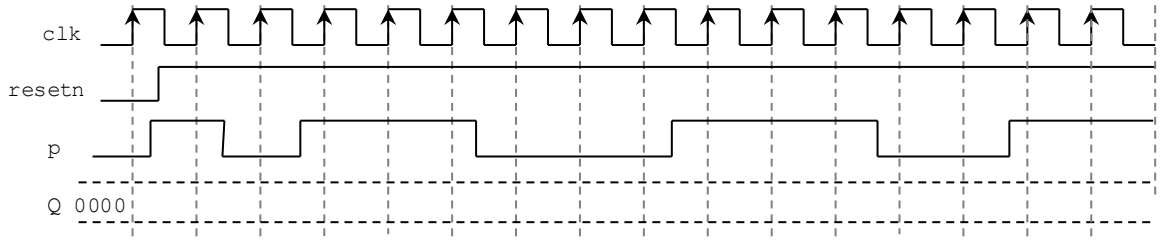
- Complete the timing diagram of the circuit whose VHDL description is shown below: (6 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( prn, a , clk: in std_logic;
         q: out std_logic);
end circ;

architecture t of circ is

   signal qt: std_logic;

begin
   process (prn, clk, x, a)
   begin
     if prn = '0' then
         qt <= '1';
      elsif (clk'event and clk = '0') then
         if x = '1' then
             qt <= a xnor (not qt);
         end if;
      end if;
   end process;
   q <= qt;
end t;
```



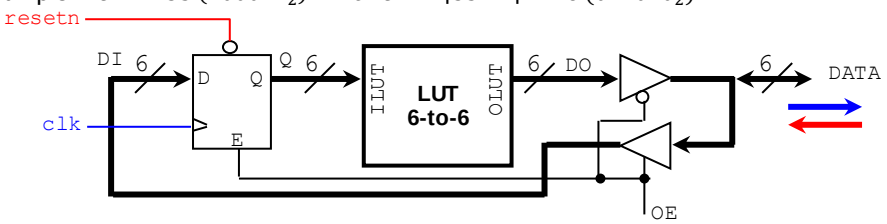
- The following circuit is a single-input compressor circuit (SIC), a component in Built-in Self-Test systems. Complete the timing diagram of the following circuit: $Q = Q_3Q_2Q_1Q_0$ (10 pts)

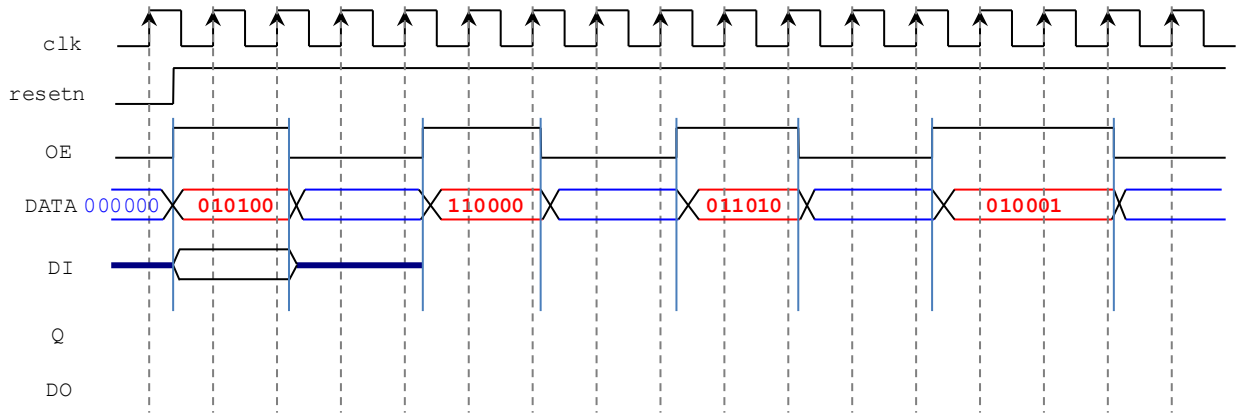




PROBLEM 3 (18 PTS)

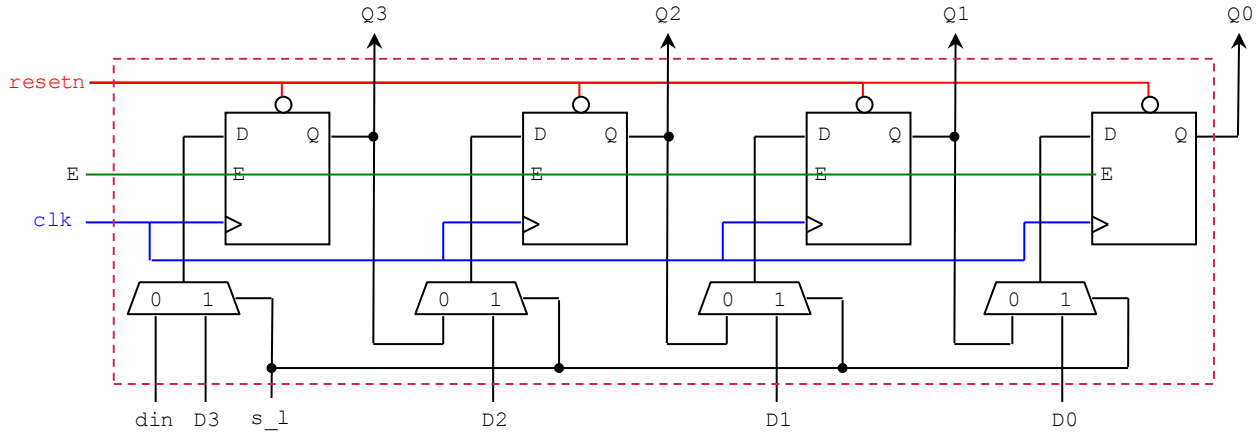
- Given the following circuit, complete the timing diagram (signals DO, Q and $DATA$).
  The LUT 6-to-6 implements the following function: $OLUT = \lceil ILUT^{0.91} \rceil$, where $ILUT$ is an unsigned number.
  For example $ILUT = 35\ (100011_2) \rightarrow OLUT = \lceil 35^{0.91} \rceil = 26\ (011010_2)$

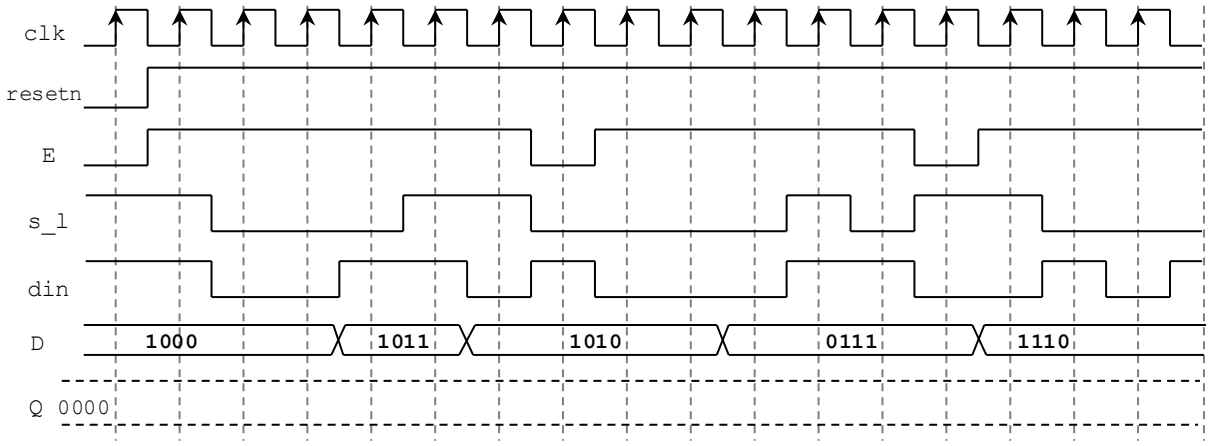




PROBLEM 4 (12 PTS)

- Complete the timing diagram of the following 4-bit parallel access shift register with enable input. Shifting operation: `s_l=0`. Parallel load: `s_l=1`. Note that $Q = Q_3Q_2Q_1Q_0$. $D = D_3D_2D_1D_0$





PROBLEM 5 (25 PTS)

- For the following circuit, do: $R = R_3R_2R_1R_0$. $G = G_3G_2G_1G_0$
  - ✓ Write structural VHDL code. Create two files: i) flip flop, ii) top file (where you will interconnect the flip flops and the logic gates). Provide a printout. (10 pts)
  - ✓ Write a VHDL testbench according to the timing diagram shown below. Complete the timing diagram by simulating your circuit (Behavioral Simulation). The clock frequency must be 100 MHz with 50% duty cycle. Provide a printout. (15 pts)